International Journal of Students' Research in Technology & Management
Vol 3 (02), February 2014, ISSN 2321-2543, pg 269-272

AN EFFICIENT IMPLEMENTATION OF BUILT IN SELF DIAGNOSIS FOR LOW POWER TEST PATTERN GENERATOR

N.Nithya # [1], M.Chandraman*[2]. S.Veerakumar*[3]

PG Scholar (ME- VLSI DESIGN) Department of ECE, Knowledge Institute of technology, Salem, India.
** Assistant Professor Department of ECE, Knowledge Institute of technology, Salem, India.*
[1]nithi.sds@gmail.com

ABSTRACT-- A New architecture of Built-In Self-Diagnosis is presented in this project. The logic Built-In-Self-Test architecture method is extreme response compaction architecture. This architecture first time enables an autonomous on-chip evaluation of test responses with negligible hardware overhead. Architecture advantage is all data, which is relevant for a subsequent diagnosis, is gathered during just one test session. Due to some reasons, the existing method Built-In Self-Test is less often applied to random logic than to embedded memories. The generation of deterministic test patterns can become prohibitively high due to hardware overhead. The diagnostic resolution of compacted test responses is in many cases poor and the overhead required for an acceptable resolution may become too high. Modifications in Linear Feedback Shift Register to generate test pattern with security for modified Built-In-Self-Test applications with reduced power requirement. The modified Built-In-Self-Test circuit incorporates a fault syndrome compression scheme and improves the circuit speed with reduction of time.

Index Terms: Logic Built In Self-Test (BIST), Fault diagnosis, Bit Swapping-Linear Feedback Shift Register(BS-LFSR),Data Encryption Standard (DES),Test Pattern Generation.

I. INTRODUCTION

VLSI Plays a major role in IC manufacturing and it needs testing of circuits. In VLSI testing, power consumption and area reduction is the major issue where it can be reduced by the method of generating the test pattern using pseudorandom pattern generator with low transition.

Baloji Naik.B described the, system of bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 × 1 multiplexer. it reduces the overall switching activity in the circuit under test during test applications. The BS-LFSR is combined with a check chain-ordering algorithm that orders the cells in a way that reduces the average and peak power (check and capture) in the test cycle or while checking out a response to a sign pattern analyzer[1].

Chethan. J designed a low power Test Pattern Generator using modifying Linear Feedback Shift Register is proposed to produce low power test vectors. The resulted low power test vectors are deployed on CUT to obtain fault coverage. The experimental results demonstrate significant power reduction by low power TPG than compared to standard LFSR [4].

Divya.E had been used pseudorandom built-in-self-test (BIST) generators that widely utilized to test integrated circuits and systems [5]

Kavya V used the sub-micron technology in FPGA to yield low power but it increased the faults[6].

Lubna Naim used bit-swapping LFSR reduced the internal transition activity probability which directly affects the dissipation of power in CUT without affecting the fault coverage [7].

Ramakrishna Porandla described that BS-LFSR is combined with a scan-chain-ordering algorithm that orders the cells in a way that reduces the average and peak power in the test cycle or while scanning out a response to a signature analyzer[10].

II. METHODOLOGY

Built-In Self-Test (BIST) has several advantages over external test: Low cost testers can be employed to apply the test, the at-speed capability of BIST enables a high throughput, a high defect coverage is achievable even for defects not explicitly targeted by the test set, and the architecture can be reused in the field . However, for random logic, BIST is not often employed as it entails some non-trivial problems:

1) The hardware overhead for the generation of deterministic test patterns can become prohibitively high.

2) The diagnostic resolution of compacted test responses is in many cases poor, and the overhead required for an acceptable resolution may become too high.

The non-shaded blocks in Fig. 1 show a generic BIST structure for pseudo-random BIST. During a BIST session a series of pseudo-random patterns is generated, applied and the corresponding test responses are compacted into a single signature, which is downloaded to the tester and compared with a reference signature.

For most designs, it is necessary to generate additional deterministic patterns in order to achieve a high defect coverage. In that case, a test pattern memory has to be implemented on chip. It corresponds to the horizontally shaded block in Fig. 1. In the last few years there has been continuous progress in encoding of deterministic pattern sets [2], [3], [4]. Today encoding methods are available, which reduce the pattern memory to an acceptable size even for large industrial designs [5].In this paper, a modification of the BIST architecture is developed, which for the first time allows to store the test responses for each test pattern on chip in a response and fail memory(vertically shaded blocks in Fig.1)

It thereby enables a stop-on-n th-fail diagnosis for random logic in the same way as it is widely used for embedded memories. The response memory contains the expected signatures for each test pattern, the fail memory contains the first n test signatures deviating from the expected signatures. Core of the architecture is a compactor, which generates extremely short signatures for each test pattern. Consequently, fail and response memory only need negligible chip area compared to the pattern memory.

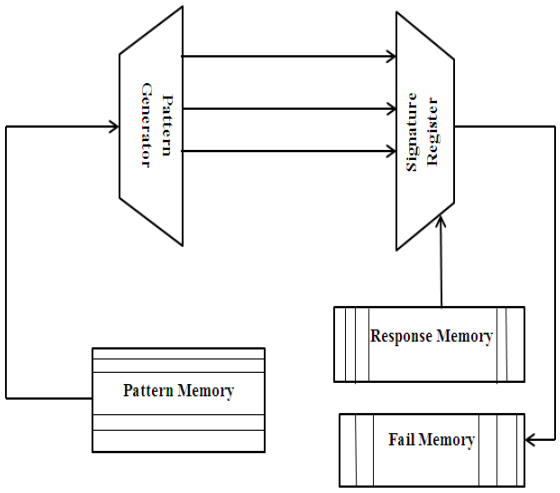


Fig.1 Generic BIST structure extended by deterministic patterns and BISD hardware

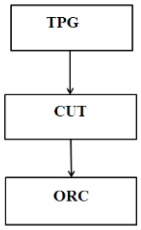
To circumvent aliasing and poor diagnostic resolution due to the short signatures, the BISD architecture is supplemented with a dedicated automatic test generation method (ATPG) and a statistical diagnosis algorithm, which is able to identify faults even if the test responses are compacted. As a result, the diagnostic success of the combined approach is even higher than that of external testing.

The new BISD scheme collects all the required diagnostic data during a single test run and stores it on chip. It has no drawback on the test flow and test time and allows complete analysis of responses during volume test, multi-site test or in-field test.

Logic BIST

Logic built-in self-test (or LBIST) is a form of built-in self-test (BIST) in which hardware and/or software is built into integrated circuits allowing them to test their own operation, as opposed to reliance on external automated test equipment.

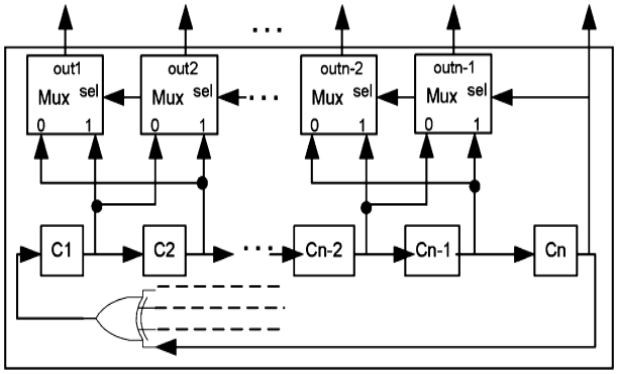
The main advantage of LBIST is the ability to test internal circuits having no direct connections to external pins, and thus unreachable by external automated test equipment. Another advantage is the ability to trigger the LBIST of an integrated circuit while running a Built. In Self-Test or power-on self-test of the finished product.



Logic BIST Architecture

ARCHITECTURE OF BS-LFSR

Bit-Swapping LFSR is based on some observations depending upon number of transition produced by LFSR at the output. In modified form of normal LFSR we used swapping property between every pair of adjacent cells of normal LFSR to design Bit-Swapping LFSR.



General architecture of Bit Swapping LFSR

General observation for LFSR- For any n-bit maximal-length LFSR that starts with any seed and runs for 2n clock cycles until it returns to the starting seed value, then the total number of transitions Ttotal that occurs is given by the formula in equation (1):

$$T_{total} = n \times 2(n-1) \qquad (1)$$

Observation for swapping Bits in BS-LFSR- If we take an example of any n-bit maximal length LFSR (n>2) and modified this LFSR for swapping arrangement, we consider one of its outputs (say bit n- the last bit) to be a selection line that will swap two neighboring bits elsewhere in the LFSR at specific value of selection line. If we set the value of selection line at 0 for swapping then n is odd and bit n =0, bit 1 will be swapped with bit 2, bit 3 with bit 4…bit n-2 with bit n-1. If n is even and bit n =0, then bit 1 will be swapped with bit 2, bit 3 with bit 4,……bit n-3 with bit n-2, in all cases the selection line (n bit) has no effect on swapping operation. If bit n =1, then no swapping is performed. In this case:

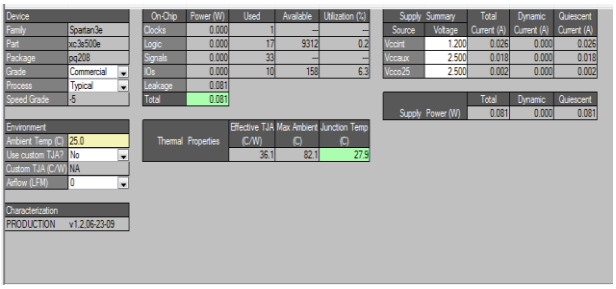
1. Modified LFSR will be generate exactly same as normal (unmodified) LFSR. Order of generated test pattern by modified LFSR will be different.

2. Swapping arrangement will save a number of transitions, swapped bits will save number of transition equal to T_{Saved} = 2(n-2). In contrast, in general observation two bits (un-swapped bits) originally produced 2 x 2(n-1) so after swapping the swap bit will therefore save T_{Saved} = 2(n-2)/ (2x 2(n-1) =25%.

APPLICATIONS

16 bit carry look ahead adder is used as a testing circuit. It consists of full adders. These full adders are tested and diagnosis where stuck at 0 and stuck at 0 fault can be tested. Xilinx software is used as a simulation tool.

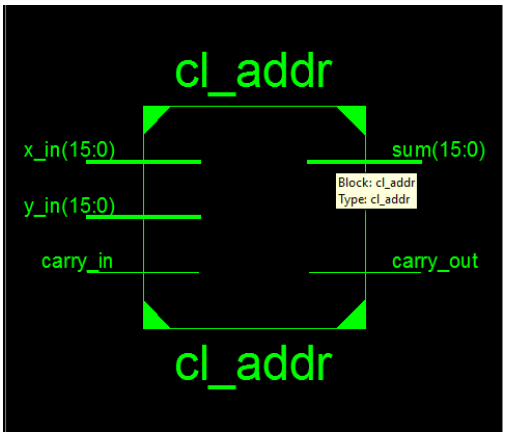
III RESULTS AND DISCUSSION



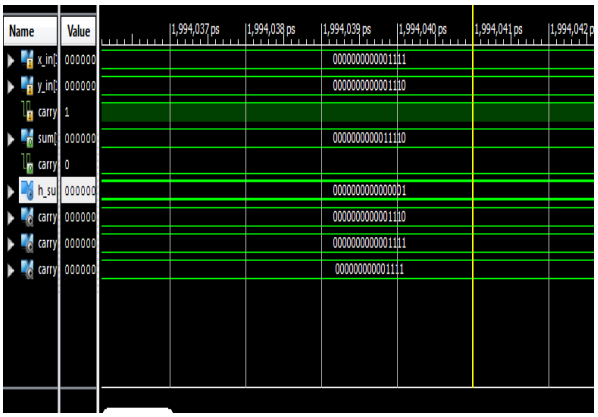
Power Analysis Result

TPG	Total Power Consumption
Normal LFSR	38 %
Modified LFSR	34 %

Simulation Results



RTL Schematic of Carry Look Ahead Adder



Results of Carry Look Ahead Adder

IV.CONCLUSION

In this paper BS-LFSR and Logic BIST was analyzed. Modified LFSR consumes less power and test patterns are generated. BISD Hardware uses less significant area demonstrate the results with minimal time duration, testing speed is high and it improves the fault coverage.

FUTURE WORK

Furthermore, Modified BS-LFSR is combined with Data Encryption Standard for security purpose.

REFERENCES

[1] Baloji Naik.B, Dr.V.Venkata Rao,(2012)"Peak- and Average-Power Reduction in Check-Based BIST by using Bit-Swapping LFSR and Check-Chain Ordering" IOSR Journal of Computer Engineering,ISSN: 2278-0661 Volume 4, Issue 4, PP 36-42.

[2] Bala Souri.K, K.Hima Bindu, K.V. Ramana Rao (2011)"A Built-In Self-Repair Scheme for Random Access Memories with 2-D Redundancy". International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-1, Issue-5.

[3] Chiraz Khedhiri1, Mouna Karmani1 and Belgacem Hamdi(2011) "A BIST Generator CAD Tool for Numeric Integrated Circuits" International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.2.

[4] Chethan J, Manjunath Lakkannavar(2013) "Design of Low Power Test Pattern Generator using Low Transition LFSR for high Fault Coverage Analysis" I.J. Information Engineering and Electronic Business, , 2, pp-15-21.

[5] Divya.E1, Prof.S.Arumugam(2013) "High Speed and Low Power implementation of 3-Weight Pattern Generation Based on Accumulator" International Journal of Advanced Research in Computer and Communication Engineering Vol. 2, Issue 2.

[6] Lubna Naim, Tarana A. Chandel,(2014) "Design of Low Transition Pseudo-Random Pattern Generator for BIST Applications"International Journal of Computer Application(0975-8887)Volume 87-No. 1.

[7] Praveen Kumar Aggarwal, Vandana Yadav, Dr. Arti Noor, "DFT (Design for Testability) Pattern Generation Task for Circuit Under Test" International Journal of Engineering Research and Applications Vol. 1, Issue 2, pp.190-193.

[8] Praveen J M N Shanmukhaswamy (2012) " Power Reduction Technique in LFSR using Modified Control Logic for VLSI Circuit" Special Issue of International Journal of Computer Applications (0975 – 8887) International Conference on Electronic Design and Signal Processing.

[9] Ramakrishna Porandla, Gella Ravikanth, Podili Ramu (2013) "Power Optimization In Digital Circuits Using Scan-Based BIST" International Journal of Research in Computer an Communication Technology, Vol 2, Issue 6,

[10] Rani Varghese ,V.Magudeeswaran,(2014) "VLSI Implementation of Test Pattern Generator for Built in self Test", I J I P A:ISSN 0975-8178,pp.61-65.